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| 09/928,011 | 08/10/2001 | Holger Sedlak | 1999P1177 | 7290 |

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| EXAMINER | |
|---|---|
| RIZZUTO, KEVIN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/928,011 | SEDLAK ET AL. | |
| | Examiner | Art Unit | |
| | Kevin P Rizzuto | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08/10/2001, 09/24/2001, and 01/23/2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/10/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-7 have been examined.

2. Acknowledgement of the following papers filed: The Information Disclosure Statement on 9/24/2001 and the Oath or Declaration and Foreign Priority Papers on 1/23/2002. The papers filed have been placed on record.

### *Priority*

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. PCT/DE00/00291, filed on 02/01/2000, which claims priority to German Application 19905510.6, filed on 02/10/19999.

### *Drawings*

4. The drawings are objected to under 37 CFR 1.83(a) because a spelling error in figure 2 ("lenght").

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the offset of claim 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method of relative addressing for a processor with multiple assembly languages.

8. Claims 1 and 2 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites the limitation "each case" in line 2. There is insufficient antecedent basis for this limitation in the claim. No "cases" are previously mentioned. For the remainder of the examination, "each case" will be interpreted as when a parameter has a particular value.

***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 3 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson and Hennessy.

12. As per claims 3 and 4, Patterson and Hennessy disclose:

- A microprocessor for processing various assembler codes: ("Assembly code" is a synonym for "assembler code" (IEEE Dictionary) and is defined as "computer instructions and data definitions expressed in a form that can be recognized and processed by an assembler." (IEEE dictionary) An assembler is "a program that translates a symbolic version of an instruction into the binary version"(Glossary of Patterson and Hennessy)

Figure 5.33 of page 383 in Patterson and Hennessy, discloses a "Multicycle datapath for MIPS handles the basic instructions" and is further described below figures 5.31 and figure 5.32. An assembler translates various assembly codes into various basic binary instructions for said multicycle datapath microprocessor. Therefore, a multicycle datapath for MIPS that handles various basic instructions is handling various assembly codes.

- A multiplexer having a first input a second input for receiving a zero value (Figure 5.48, page 414; and figure 5.34, p384. Whenever an operation involving the ALU occurs, such as an add, the four-input multiplexer that has an output to the ALU is used. If there is a zero stored in the specified register in the instruction for SrcB, and when ALUSrcB is set to "00", the multiplexer will have a zero value as an input)

-A third input receiving a parameter designating a respective assembler code: (Figure 5.48, page 414, ALUSrcB is a parameter that will indicate what type of assembler code is being executed when said multiplexer is in use, for example, it will be set accordingly when an add type assembler code is used or a branch type assembler code (page 386)).

- A memory for storing an instruction length and having an output connected to said first input of said multiplexer: (Memory is defined as "All the addressable storage in a processing unit and other internal storage that is used to execute instructions"(IEEE dictionary) Figure 5.48, page 414, said multiplexer has a "4" as an input. It is inherent that the "4" must

be stored in a memory. In order for the "4" to exist in the datapath, there must be some form of internal storage and it is used to execute instructions. Also, the "4" is an instruction length for the MIPS instruction set in the understanding that the program counter is incremented by "4" to get to the next sequential instruction, moving the program counter one instruction length ahead in memory.

- Depending on how the parameter is set, a different relative addressing takes place: (Figure 5.48, page 414, ALUSrcB is a parameter that will indicate which input is selected for the ALU to calculate the next program counter value. If there is a branch code, the ALUSrcB parameter will select "11" to indicate to add a value specified in the code to the current program counter address. If it is an R-type code, for example, the ALUSrcB will select the "4" input to the multiplexer to be added to the current program counter (back inside cover). Therefore there is different relative addressing occurring depending on the parameter.

- A program counter (Figure 5.48, page 414, labeled "PC")

- A computation unit for computing relative addresses: (Figure 5.48, page 414; Figure 5.34, page 384; The four input multiplexer with signal "PCSource" uses the input (PCSource) to compute an output (relative address) for the program counter)

- An addition unit (as in claim 3) and a subtraction unit (as in claim 4) connected between said program counter and said computation unit:

(Figure 5.48, page 414 shows an "ALU" that has a program counter input (PC) when ALUSrcA is a "0" and has an output to said computation unit.) - Said adding unit having a first input connected to said program counter, a second input connected to said multiplexer an output connected to said computation unit: (Figure 5.48, page 414 shows an "ALU" that has a program counter input (PC) when ALUSrcA is a "0", said four input multiplexer (with signal ALUSrcB) and has an output to said computation unit.) The ALU is both an addition unit and a subtraction unit. (Figure 5.34, Page 384; ALUOp = 00 indicates an add op, ALUOp = 01 indicates a subtract op), therefore it is an addition unit and a subtraction unit.

***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1, 2, 5, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hauris, U.S. Patent 7,821,183 and further in view of Patterson and Hennessy (Computer Organization, The Hardware/Software Interface 2nd Edition).

15. As per claim 1, Hauris discloses a microprocessor for processing various assembler codes comprising:

-A plurality of program counters: (Abstract, Column 3, lines 34-35; Column 4, lines 16-41; Figure 2, items 22 and 30)

16. While Hauris does disclose instructions that will be translated to assembler codes and parameters, he does not teach the assembly codes and parameters directly. He also fails to specifically teach a parameter designating a respective assembler code and depending on how the parameter is set, a different relative addressing takes place, and also dependent on the parameter, one of said program counters is active in a computation of relative addresses.

17. Patterson and Hennessy disclose:

-Multiple assembler codes being processed: (Back inside cover shows many different assembler codes and Figure 5.48, page 414 shows a processor to execute the assembler codes)

-A parameter designating a respective assembler code: (Back inside cover, the parameter being the op-code which is in the op-field)

-Depending on how the parameter is set, a different relative addressing takes place (back inside cover and p. 380; The assembler code "bne" contains the parameter that instructs the processor to do a PC-relative branch if a condition is met. A PC-relative branch uses a branch offset, included in the assembler code, to add to the current program counter. Also, assembler codes such as the R-type "add" contain the parameter that designates the program counter to be updated by just adding four to the current address in the program counter (page 385). Therefore, two

types of relative addressing occur, a PC-relative branch and when four is added to the current program counter, depending on the parameter.

-Dependent on the parameter, one of said program counters is active in a computation of relative addresses: (Column 4, lines 16-41; Back inside cover; when the parameter dictates a subroutine call or return (jal or jr in assembler code), a program counter is activated and another is deactivated, and as stated before, the current program counter is used in the different types of relative addressing)

18. While the base reference discloses a microprocessor with multiple program counters and instructions to switch between the program counters, it never states the instruction set to be used. It would be obvious to one of ordinary skill in the art that the MIPS instruction set would be chosen as the instruction set to be used because it is well known and popular in the art, as is disclosed in Patterson and Hennessy. "The chosen instruction set comes from MIPS, used by NEC, Nintendo, Silicon Graphics, and Sony, among others, and is typical of instructions set designed since the early 1980s." (p. 107, top paragraph) Choosing the popular and proven instruction set MIPS would make the base reference compatible with existing assemblers and since it is well known in the art, it would be easier for individuals in the art to understand and work with the processor.

19. It would be obvious to one of ordinary skill in the art that the above mentioned advantages would have provided the motivation to implement the MIPS instruction set on the base reference's processor.

20. As per claim 2, Hauris, in view of Patterson and Hennessy, disclose a microprocessor comprising:

-A computation unit: (Hauris, Figure 2, item 16 is the computer memory, Item 26 is the instruction unit, and the instruction unit has outputs going "to processor", the combination of said items are a type of computation unit)

-A multiplexer connected to said program counters (Hauris, Figure 2, item 32):

-Said multiplexer receives and is controlled by the parameter: (Hauris, Figure 2 shows the parameter as the input to items 22 and 30 into the CNT input and to the multiplexer input 2, the operation of the parameter is disclosed in column 4, lines 5-41; It is stated that the parameter turns on one program counter and turns off another when it designates a "subroutine call" or "subroutine return" instruction. CNT is part of the decoded parameter.

-Said multiplexer having an output connected to said computation unit for the relative addresses (Hauris, Figure 2, item 32 is directly connected to item 16, part of the computation unit)

21. As per claim 5, Hauris discloses a method of relative addressing in a microprocessor with steps comprising:

-Providing a plurality of program counters for various operating states and assembler codes: (Abstract, Column 3, lines 34-35; Column 4, lines 16-41)

22. While Hauris does disclose instructions that will be translated to assembler codes and parameters, he does not teach the assembly codes and parameters directly. He also fails to disclose a step of determining relative addresses in dependence on one of an operating state and a parameter for a respective assembler code. He also fails to disclose a step of selecting one of the program counters for use in determining the relative addresses in dependence on one of the operating state and the respective assembler code.

23. Patterson and Hennessy disclose:

-Determining relative addresses in dependence on one of an operating state and a parameter for a respective assembler code: (back inside cover and p. 380; The assembler code "bne" contains the parameter that instructs the processor to do a PC-relative branch if a condition is met. A PC-relative branch uses a branch offset, included in the assembler code, to add to the current program counter. Also, assembler codes such as the R-type "add" contain the parameter that designates the program counter to be updated by just adding four to the current address in the program counter (page 385). Therefore, two types of relative addressing occur, a PC-relative branch and when four is added to the current program counter, depending on the parameter.

-Selecting one of the program counters for use in determining the relative addresses in dependence on one of the operating state and the respective assembler code: (Column 4, lines 16-41; Back inside cover; when the parameter dictates a subroutine call or return (jal or jr in assembler code),

a program counter is activated and another is deactivated, and as stated before, the current program counter is used in the different types of relative addressing)

24. While the base reference discloses a microprocessor with multiple program counters and instructions to switch between the program counters, it never states the instruction set to be used. It would be obvious to one of ordinary skill in the art that the MIPS instruction set would be chosen as the instruction set to be used because it is well known and popular in the art, as is disclosed in Patterson and Hennessy. "The chosen instruction set comes from MIPS, used by NEC, Nintendo, Silicon Graphics, and Sony, among others, and is typical of instructions set designed since the early 1980s." (p. 107, top paragraph) Choosing the popular and proven instruction set MIPS would make the base reference compatible with existing assemblers and since it is well known in the art, it would be easier for individuals in the art to understand and work with the processor.

25. It would be obvious to one of ordinary skill in the art that the above mentioned advantages would have provided the motivation to implement the MIPS instruction set on the base reference's processor.

26. As per claim 6, Hauris in further view of Patterson and Hennessy disclose:

-Performing one of an addition and a subtraction of an instruction length to/from a program counter reading for a relative address computation in dependence on one of the various operating states and the assembler codes: (Figure 5.48, page 414 and the back inside cover, when an R-type

assembler code is executed, the program counter is incremented by 4. The "4" is an instruction length for the MIPS instruction set in the understanding that the program counter is incremented by "4" to get to the next sequential instruction, moving the program counter one instruction length ahead in memory.)

-Leaving the program counter reading unchanged: (Patterson and Hennessy, page 386-387; The program counter is updated when the translated assembly code is a branch instruction, during the execution stage. The program counter is unchanged during the execution stage if the assembly code being executed is an R-type instruction.)

27. As per claim 7, Hauris in further view of Patterson and Hennessy disclose:

-Performing one of an addition and a subtraction of the instruction length to/from an offset value used for the computation of the relative addresses in dependence on one of the various operating states and the assembler codes: (The program counter is an offset from the base address that is used for computing the relative address. When an assembly code is translated into a R-type instruction, during its execution, a "4" (instruction length) is added to the program counter. This forms a new relative address that is then loaded into the program counter register.

-Leaving the offset value unchanged: (Patterson and Hennessy, page 386-387; The program counter is updated when the translated assembly code is a branch instruction, during the execution stage. The program

counter is unchanged during the execution stage if the assembly code being executed is an R-type instruction.)

***Conclusion***

28. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (703)305-6783. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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